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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary SUPPLEMENTAL	Application No. 10/802,566	Applicant(s) LIN, MOU-SHIUNG	
	Examiner Ajay K. Arora	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/4/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33,40-51 and 76-89* is/are pending in the application.

4a) Of the above claim(s) *4,29,30,32,33 and 46* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-28,31,40-45,47-51 and 76-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Supplemental Action

In the previous office action, an incorrect PTO-892 was sent out. This supplemental action provides the correct PTO-892 – References Cited By the Examiner. Please note that the references cited within the Detailed Action were correct and therefore, the only change is the correction to PTO-892.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 9, 15, 40, 76 and 83 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The above said claims recite "a transistor in and on said semiconductor substrate" (emphasis added). It is not clear how "a transistor", which appears to refer to a single transistor can be simultaneously "in and on" the semiconductor substrate. For the purpose of this office action, it will be assumed that as long as a transistor is formed on a semiconductor substrate (which is typical for integrated circuit chips), it can be interpreted as "a transistor in and on said

semiconductor substrate". In other words, any integrated circuit chip comprising a semiconductor substrate can be considered to have "a transistor in and on said semiconductor substrate".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 7, 9, 13, 14, 40-45, 49-50, 83-87 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6,303,423), hereinafter Lin.

Regarding claim 1, Lin (refer to Figure 1) teaches a circuit component comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 25-29);

a power bus (comprising 26 or 28) over said semiconductor substrate (Col. 8, lines 19-32);

a ground bus (comprising 26 or 28) over said semiconductor substrate (Col. 8, lines 19-32),

an electronic component over said semiconductor substrate (Col. 8, lines 10-17);

a first connection (to 26 or 28) connecting said electronic component to said power bus ; and

a second connection (to 26 or 28) connecting said electronic component to said ground bus.

However, the embodiment of Figure 1 of Lin does not clearly state that the electronic component is specifically "a capacitor" and that the connections to the power bus and ground bus is by "solder" connections. The embodiment of Figure 10 of Lin utilizes a substrate similar to that of Figure 1, wherein the electronic component (54) over said semiconductor substrate (10) may be a capacitor (Col. 14, lines 22-23), and the connections (52) of the capacitor are solder connections (Col. 14, lines 16-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the electronic component is a capacitor and that the connections to the power bus and ground bus is by solder connections. The ordinary artisan would be motivated to modify Lin at least for the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24) while using an attachment material like solder which provides good adhesion at a process temperature compatible with a wide variety of circuit component manufacturing processes.

Regarding claim 2, Lin (refer to Figures 1) teaches a metallization structure (16) over said semiconductor substrate (10), and a passivation layer (18) over said metallization

structure, wherein said power and ground buses (26 or 28) are over said passivation layer (18).

Regarding claim 7, Lin does not specifically teach that said power bus may comprise gold. However, Lin teaches that points of electrical contact may comprise gold (Col. 15, lines 61-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that said power bus may comprise gold. The ordinary artisan would be motivated to modify Lin at least for utilizing a highly conductive material that has excellent resistance to corrosion.

Regarding claim 9, Lin (refer to Figure 1) teaches a circuit component comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 25-29);

a first contact pad (16) over said semiconductor substrate;

a passivation layer (18) over said semiconductor substrate, a first opening (opening through which 38 connects to 16) in said passivation layer (18) exposing a top surface of said first contact pad (16), wherein said passivation layer comprises nitride (Col. 8, lines 52-56);

a second contact pad (28) connected to said top surface, wherein the position of said second contact pad from a top perspective view is different from that of said first contact pad (because pads 16 and 28 are of different size and also their center points are not aligned); and

an electronic component over said passivation layer, wherein said electronic component is connected to said second pad (Col. 8, lines 10-17);

However, the embodiment of Figure 1 of Lin does not clearly state that the electronic component is specifically "a capacitor". The embodiment of Figure 10 of Lin utilizes a substrate similar to that of Figure 1, wherein the electronic component (54) over said semiconductor substrate (10) may be a capacitor (Col. 14, lines 22-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the electronic component is a capacitor. The ordinary artisan would be motivated to modify Lin at least for the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24).

Regarding claim 13, Lin as modified above teaches a solder (this limitation has already been addressed in claim 1 in view of embodiment of Figure 10 of Lin) connecting said capacitor to said contact pad.

Regarding claim 14, Lin teaches substantially the claimed structure but does not teach that said second contact pad comprises "gold". However, Lin teaches that points of electrical contact may comprise gold (Col. 15, lines 61-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that said second contact pad comprises gold. The ordinary artisan would be

motivated to modify Lin at least for utilizing a highly conductive material that has excellent resistance to corrosion.

Regarding claim 40, Lin (refer to Figure 1) teaches a method of fabricating a circuit component comprising:

providing a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 25-29);

a first contact pad (16) over said semiconductor substrate;

a passivation layer (18) over said semiconductor substrate, an opening (opening through which 38 connects to 16) in said passivation layer (18) exposing a top surface of said first contact pad (16); and

a second contact pad (28) connected to said top surface, wherein the position of said second contact pad from a top perspective view is different from that of said first contact pad (because pads 16 and 28 are of different size and also their center points are not aligned) and wherein said passivation layer comprises nitride (Col. 8, lines 52-56); and

mounting an electronic component over said passivation layer, wherein said electronic component is connected to said second pad (Col. 8, lines 10-17);

However, the embodiment of Figure 1 of Lin does not clearly state that the electronic component is specifically "a capacitor". The embodiment of Figure 10 of Lin utilizes a substrate similar to that of Figure 1, wherein the electronic component (54) over said

semiconductor substrate (10) may be a capacitor (Col. 14, lines 22-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the electronic component is a capacitor. The ordinary artisan would be motivated to modify Lin at least for the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24).

Regarding claim 41, Lin (refer to Figure 1) teaches substantially the claimed method but does not specifically state that forming "said second contact pad" comprises "electroplating". However, Lin teaches that forming metal interconnects may comprise electroplating (Col. 10, lines 31-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said second contact pad comprises electroplating. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature, cost effective metal deposition technique that offers high rate of deposition.

Regarding claim 42, Lin (refer to Figure 1) teaches substantially the claimed method but does not specifically state that forming "said second contact pad" comprises "electroless plating". However, Lin teaches that forming metal interconnects may comprise electroless plating (Col. 9, lines 31-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said second contact pad comprises electroless plating. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a a metal coating process

that can generally produce less porous plated metal (which is less susceptible to corrosion) compared to electroplating.

Regarding claim 43, Lin (refer to Figure 1) teaches substantially the claimed method but does not specifically state that forming "said second contact pad" comprises "sputtering". However, Lin teaches that forming metal interconnects may comprise sputtering (Col. 10, lines 38-41 and Col. 15, lines 61-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said second contact pad comprises sputtering. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a metal coating process that produces very thin films with superior adhesion (for example, compared to vapor deposition).

Regarding claim 44, Lin (refer to Figure 1) teaches substantially the claimed method but does not specifically state that forming "said second contact pad" comprises "printing". However, Lin teaches that forming metal interconnects may comprise printing (Col. 10, lines 38-41 and Col. 20, lines 21-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said second contact pad comprises printing. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature process for forming relatively thick metal pad with quick turn around and inexpensive tooling.

Regarding claim 45, the embodiment of Figure 1 of Lin as modified above in view of embodiment of Figure 10 of Lin teaches that said mounting said capacitor comprises using surface mount technology (using contact balls 52 of Figure 10), the motivation being to provide a very short interconnect for the capacitor to minimize losses.

Regarding claim 49, Lin teaches substantially the claimed method but does not specifically state that forming "said second contact pad" comprises depositing "gold". However, Lin teaches that forming metal interconnects may comprise gold (Col. 10, lines 32-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said second contact pad comprises depositing gold. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a metal with high electrical conductivity that has excellent corrosion resistance.

Regarding claim 50, Lin teaches substantially the claimed method but does not specifically state that forming "said second contact pad" comprises depositing "copper". However, Lin teaches that forming metal interconnects may comprise copper (Col. 10, lines 32-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said second contact pad comprises depositing copper. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a metal with high electrical conductivity that is significantly less expensive that gold.

Regarding claim 83, Lin (refer to Figure 1) teaches a method of fabricating a circuit component comprising:

providing a semiconductor substrate (10),

a transistor in and on said semiconductor substrate (Col. 7, lines 25-29);

a power bus (comprising 26 or 28) over said semiconductor substrate (Col. 8, lines 19-32), and a ground bus (comprising 26 or 28) over said semiconductor substrate (Col. 8, lines 19-32), and

mounting an electronic component over said semiconductor substrate (Col. 8, lines 10-17), wherein said electronic component is connected to said power and ground buses.

However, the embodiment of Figure 1 of Lin does not clearly state that the electronic component is specifically "a capacitor". The embodiment of Figure 10 of Lin utilizes a semiconductor substrate similar to that of Figure 1, wherein the electronic component (54) over said semiconductor substrate (10) may be a capacitor (Col. 14, lines 22-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the electronic component is a capacitor. The ordinary artisan would be motivated to modify Lin at least for the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24).

Regarding claim 84, Lin (refer to Figure 1) teaches substantially the claimed method including forming a contact pad connected to said power bus, but does not specifically state that forming "said contact pad" comprises "printing". However, Lin teaches that forming metal interconnects may comprise printing (Col. 10, lines 38-41 and Col. 20, lines 21-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said contact pad comprises printing. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature process for forming relatively thick metal pad with quick turn around and inexpensive tooling.

Regarding claim 85, Lin (refer to Figure 1) teaches substantially the claimed method but does not specifically state that forming "said contact pad" comprises "electroplating". However, Lin teaches that forming metal interconnects may comprise electroplating (Col. 10, lines 31-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said contact pad comprises electroplating. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature, cost effective metal deposition technique that offers high rate of deposition.

Regarding claim 86, Lin (refer to Figure 1) teaches substantially the claimed method but does not specifically state that forming "said contact pad" comprises "electroless plating". However, Lin teaches that forming metal interconnects may comprise

electroless plating (Col. 9, lines 31-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming said contact pad comprises electroless plating. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a metal coating process that can generally produce less porous plated metal (which is less susceptible to corrosion) compared to electroplating.

Regarding claim 87, the embodiment of Figure 1 of Lin as modified above in view of embodiment of Figure 10 of Lin teaches that said mounting said capacitor comprises using a surface mount technology (using contact balls 52 of Figure 10), the motivation being to provide a very short interconnect for the capacitor to minimize losses.

Regarding claim 89, the embodiment of Figure 1 of Lin as modified above in view of embodiment of Figure 10 of Lin teaches that said capacitor is connected to said power and ground buses through multiple solder (Col. 14, lines 16-21) connections (52).

Claims 3, 5, 6, 8, 10-12, 48 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Nakanishi (US 6,921,980), hereinafter Nakanishi.

Regarding claim 3, Lin (refer to Figure 1) teaches:

A contact pad (16) over said semiconductor substrate (10);

A passivation layer (18) over said semiconductor substrate, an opening (opening through which 38 connects to 16) in said passivation layer (18) exposing said contact pad (16).

However, Lin does not teach "a wirebond" on said contact pad. Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches a circuit component with a semiconductor substrate (2) with a contact pad (3) and a passivation layer (Col. 4, lines 22-24, not shown in figure) exposing said contact pad, wherein the circuit component has a wirebond (12) on the said contact pad (3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that the circuit component has a wirebond on said contact pad. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature interconnection technology like wirebonding, which is cost-effective and for which manufacturing equipment is widely available.

Regarding claim 5, Lin (refer to Figure 1) teaches:

A first contact pad (16) over said semiconductor substrate;

A passivation layer (18) over said semiconductor substrate, an opening (opening through which 38 connects to 16) in said passivation layer exposing said first contact pad;

a second contact pad (28) on said first contact pad (16).

However, Lin does not disclose "a wirebond on said second contact pad". Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches a circuit component with a semiconductor substrate (2) with a contact pad (3), comprising a wirebond (12) on said second contact pad. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that the circuit component has a wirebond on said second contact pad. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature interconnection technology like wirebonding, which is cost-effective and for which manufacturing equipment is widely available.

Regarding claim 6, Lin (refer to Figure 1) teaches:

A contact pad (16) over said semiconductor substrate (10), wherein an interconnect connects the said capacitor to the contact pad (16).

However, Lin does not teach that the above interconnect is "a wirebond on said contact pad". Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches a circuit component with a semiconductor substrate (2) with a contact pad (3), wherein interconnect is a wirebond on said contact pad. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that the interconnect is a wirebond on said contact pad. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature interconnection technology like wirebonding, which is cost-effective and for which manufacturing equipment is widely available.

Regarding claim 8, Lin (refer to Figure 1) teaches

a passivation layer (18) over said semiconductor substrate,

a contact pad (28) over said passivation layer.

However, Lin does not teach "a wirebond on said contact pad". The teaching of a wirebond on a contact pad and its associated motivation has already been addressed in claim 3 in view of Nakanishi.

Regarding claim 10, Lin (refer to Figure 1) teaches substantially the claimed structure including a third contact pad (16 – because there are multiple contact pads 16) exposed by a second opening in said passivation layer (18), but does not teach "a wirebond" on said third contact pad. The teaching of a wirebond on a contact pad and its associated motivation has already been addressed in claim 3 in view of Nakanishi.

Regarding claim 11, Lin (refer to Figure 1) teaches substantially the claimed structure including a third contact pad (26) over said passivation layer (18), but does not teach "a wirebond" on said third contact pad. The teaching of a wirebond on a contact pad and its associated motivation has already been addressed in claim 3 in view of Nakanishi.

Regarding claim 12, Lin (refer to Figure 1) teaches substantially the claimed structure comprising a third contact pad (16 – because there are multiple contact pads 16) exposed by a second opening in said passivation layer (18), a fourth contact pad (26) on said third contact pad, but does not teach "a wirebond" on said fourth contact pad.

The teaching of a wirebond on a contact pad and its associated motivation has already been addressed in claim 3 in view of Nakanishi.

Regarding claim 48, Lin (refer to Figure 1) teaches substantially the claimed integrated circuit but does not teach it further comprising forming a wirebond over said semiconductor. Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches a semiconductor component, comprising forming a wirebond over said semiconductor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to further comprise forming a wirebond over said semiconductor. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature interconnection technology like wirebonding, which is cost-effective and for which manufacturing equipment is widely available.

Regarding claim 88, Lin teaches substantially the claimed method but does not teach that "forming a wirebond over said semiconductor substrate". Nakanishi (refer to Figure 1a, 1b, 2a-2e and 3a) teaches the method of forming a circuit component with a semiconductor substrate (2), wherein the method further comprises forming a wirebond (12) over said semiconductor substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that the method further comprises forming a wirebond over said semiconductor substrate. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a mature

interconnection technology like wirebonding, which is cost-effective and for which manufacturing equipment is widely available.

Claims 15, 17-19, 21-22, 24-25, 27, 31 and 76-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Lin.

Regarding claim 15, Nakanishi (refer to Figures 1b, 2a-e and 3a and to markup of Figure 1b below) teaches a circuit component comprising:

a semiconductor substrate (2);

a transistor in and on said semiconductor substrate;

a first metal pad (see below markup of Figure 1b) over said semiconductor substrate; a second metal pad (see below markup of Figure 1b) over said semiconductor substrate, wherein said second metal pad is used to be wirebonded thereto (see Figure 3a);

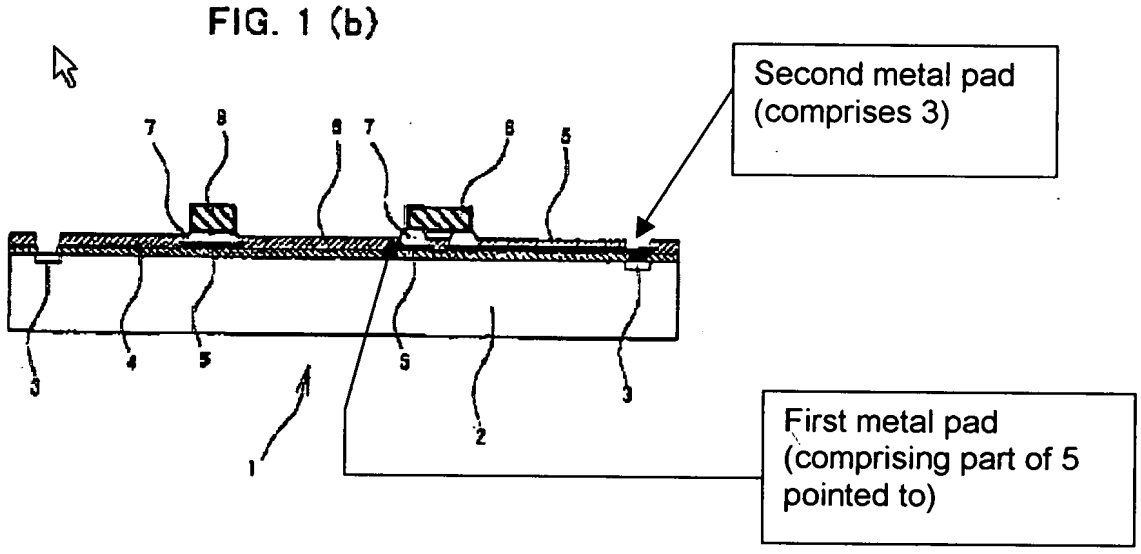
an electronic component (8) over said semiconductor substrate; and

a solder (7) connecting (Col. 4, lines 63-65) said electronic component to said first metal pad (see below markup of Figure 1b).

However, Nakanishi does not teach that the electronic component is specifically a "capacitor". Lin (refer to Figure 10) teaches a circuit component comprising a semiconductor substrate with an electronic component over said semiconductor substrate, wherein the electronic component (54) may be a capacitor (Col. 14, lines 22-

23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that the electronic component is a capacitor. The ordinary artisan would be motivated to modify Nakanishi for at least the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24).

Markup of Figure 1b of Nakanishi for Rejection of Claim 15



Regarding claim 17, Nakanishi teaches that the said first metal pad comprises gold (Col. 4, lines 58-63).

Regarding claim 18, Nakanishi teaches that said first metal pad comprises copper (Col. 4, lines 58-63).

Regarding claims 19 and 21, Nakanishi teaches substantially the claimed structure but does not teach "a ground bus connected to said capacitor" (for claim 19) or "a power bus connected to said capacitor" (for claim 21). Lin teaches that a ground bus (or a power bus) may be connected to a component, which may be a capacitor (Col. 8, lines 19-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that a ground bus (or power bus) is connected to said capacitor. The ordinary artisan would be motivated to modify Nakanishi for at least the purpose of reducing parasitics and voltage drop along the ground (or power) bus (see Lin, Col. 4, lines 47-52).

Regarding claim 22, Nakanishi (refer to Figures 1b, 2a-e and 3a) teaches a first metallization structure (comprising 3) over said semiconductor substrate (2), a passivation layer (Col. 4, lines 22-24, not shown in figure) over said first metallization structure, and a second metallization structure (comprising 5) over said passivation layer, wherein said second metallization structure is provided with said first metal pad (see markup of Figure 1b of Nakanishi above).

Regarding claim 24, Nakanishi (refer to Figures 1b, 2a-e and 3a) teaches a first metallization structure (comprising 3) over said semiconductor substrate (2), a

passivation layer (Col. 4, lines 22-24, not shown in figure) over said first metallization structure, and a second metallization structure (comprising 5) over said passivation layer, wherein said second metallization structure is provided with said second metal pad (see markup of Figure 1b of Nakanishi above).

Regarding claim 25, Nakanishi (refer to Figures 1b, 2a-e and 3a) teaches a passivation layer (Col. 4, lines 22-24, not shown in figure) over said semiconductor substrate (2), wherein said second metal pad (comprises 3, see markup of Figure 1b of Nakanishi above) is exposed by an opening in said passivation layer and wherein said passivation layer comprises nitride (Col. 4, lines 22-24).

Regarding claims 27, Nakanishi (refer to Figures 1b, 2a-e and 3a), teaches substantially the claimed structure but does not specifically state that "said second metal pad comprises gold". Lin teaches that metal interconnects may comprise gold (Col. 10, lines 32-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that said second metal pad comprises gold. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of utilizing a metal with high electrical conductivity that has excellent corrosion resistance.

Regarding claim 31, Nakanishi (refer to Figures 1b, 2a-e and 3a) teaches a first metallization structure (comprising 3) over said semiconductor substrate (2), a passivation layer (Col. 4, lines 22-24, not shown in figure) over said first metallization

structure, a second metallization structure (comprising 5) over said passivation layer, and a polymer layer (6) over said second metallization structure, wherein said second metallization structure is provided with said first metal pad, and an opening in said polymer layer exposes said first metal pad.

Regarding claim 76, Nakanishi (refer to Figures 1b, 2a-e and 3a and to markup of Figure 1b provided below) teaches a method of fabricating a circuit component comprising:

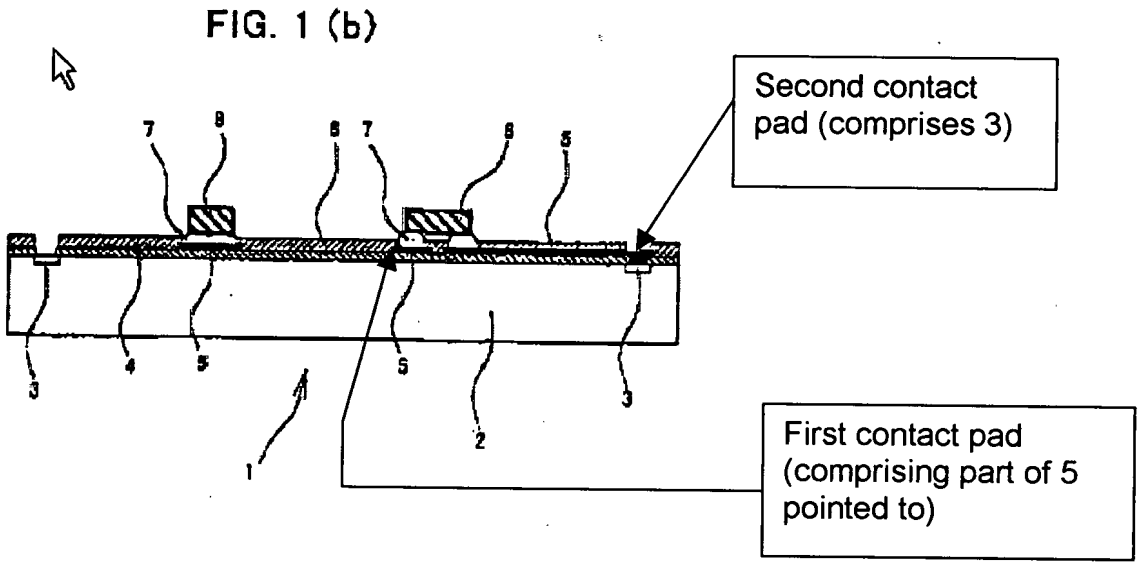
providing a semiconductor substrate (2), a transistor in and on said semiconductor substrate, a first contact pad (see Figure 1b markup) over said semiconductor substrate, a second contact pad (see markup of Figure 1b) over said semiconductor substrate, wherein said second contact pad is used to be wirebonded thereto (see Figure 3a); and

mounting an electronic component (8) over said semiconductor substrate; wherein said electronic component is connected to said first contact pad (see markup of Figure 1b).

However, Nakanishi does not teach that the electronic component is specifically a "capacitor". Lin (refer to Figure 10) teaches a circuit component comprising a substrate with an electronic component over said semiconductor substrate, wherein the electronic component (54) may be a capacitor (Col. 14, lines 22-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that the electronic component is a capacitor. The ordinary artisan would be

motivated to modify Nakanishi for at least the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24).

Markup of Figure 1b of Nakanishi for Rejection of Claim 76



Regarding claim 77, Nakanishi teaches substantially the claimed method but does not specifically state that forming "said first contact pad" comprises "printing". However, Nakanishi teaches that forming metal interconnects may comprise printing (Col. 4, lines 63--65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that forming said first contact pad comprises printing. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of utilizing a mature process for forming relatively thick metal pad with quick turn around and inexpensive tooling.

Regarding claim 78, Nakanishi teaches substantially the claimed method but does not specifically state that forming "said first contact pad" comprises "electroplating". However, Nakanishi teaches that forming metal interconnects may comprise electroplating (Col. 3, lines 44-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that forming said first contact pad comprises electroplating. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of utilizing a mature, cost effective metal deposition technique that offers high rate of deposition.

Regarding claim 79, Nakanishi teaches substantially the claimed method but does not specifically state that forming "first contact pad" comprises "electroless plating". Lin teaches that forming metal interconnects may comprise electroless plating (Col. 9, lines 31-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that forming said second contact pad comprises electroless plating. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of utilizing a a metal coating process that can generally produce less porous plated metal (which is less susceptible to corrosion) compared to electroplating.

Regarding claim 80, Nakanishi (refer to Figure 1b), as modified above of so that the electronic component (8) is a capacitor, teaches that said mounting said capacitor comprises using surface mount technology (using 7 of Figure 1b).

Regarding claim 81, Nakanishi (refer to Figure 1b and 3a) teaches that the method further comprises forming a wirebond (12) connected to said second contact pad.

Regarding claim 82, Nakanishi, as modified above of so that the electronic component (8) is a capacitor, teaches that said capacitor (8) is connected to said first contact pad through a solder (7, see Col. 4, lines 63-67).

Claims 16, 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Lin, and further in view of Murdeshwar (6,267,290), hereinafter Murdeshwar.

Regarding claims 16, Nakanishi (refer to Figures 1b, 2a-e and 3a), teaches the circuit component further comprising a wirebond (12) on said second metal pad (see markup of Figure 1b). However, Nakanishi does not teach that said wirebond comprises "gold". Murdeshwar teaches wirebonding wherein wirebonds comprise gold (Col. 5, lines 2-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that the wirebond comprises gold. The ordinary

artisan would be motivated to modify Nakanishi at least for the purpose of providing a wire bond material that is resistant to oxidation (Col. 5, lines 4-6).

Regarding claim 20, Nakanishi as modified above by Lin teaches that said capacitor is connected to said wirebond (12).

Regarding claim 23, Nakanishi (refer to Figures 1b, 2a-e and 3a) teaches a first metallization structure (comprising 3) over said semiconductor substrate (2), a passivation layer (Col. 4, lines 22-24, not shown in figure) over said first metallization structure, and a second metallization structure (comprising 5) over said passivation layer, wherein said capacitor (8, as modified by Lin) is connected to said wirebond (12) through said second metallization structure (comprising 5).

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Lin, and further in view of Greer (US 6,451,681), hereinafter Greer.

Regarding claim 26, Nakanishi (refer to Figures 1b, 2a-e and 3a) teaches a third metal pad (see see markup of Figure 1b of Nakanishi below) over said semiconductor substrate (2), and a passivation layer (Col. 4, lines 22-24, not shown in figure) over said semiconductor substrate (2), an opening in said passivation layer exposing said third metal pad, wherein said wherein passivation layer comprises nitride. However, Nakanishi does not teach the claimed position of the pad; i.e. Nakanishi does not teach

that "said second metal pad is on said third metal pad". Greer teaches (refer to Figure 4) a metal pad (312) which is on another metal pad (122/124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that said second metal pad is on said third metal pad. The ordinary artisan would be motivated to modify Lin at least for the purpose of providing a second metal pad (which is wirebond thereto per claim 15) that provides a composition more suitable than third metal pad for adhesion and integrity of the interconnect for the specific wirebonding material/process used (Col. 5, lines 21-33).

Claims 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Lin, and further in view of Thomas (US 5,346,858), hereinafter Thomas.

Regarding claim 28, Nakanishi teaches substantially the claimed structure but does not teach that the said second metal pad "comprises aluminum". Thomas teaches a semiconductor device wherein a metal pad comprises aluminum (Col. 2, lines 34-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made so that said second metal pad comprises aluminum. The ordinary artisan would be motivated to modify Nakanishi at least for the purpose of providing a bond pad material with high conductivity which is not as expensive as other high conductivity materials like copper.

Claims 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Greer (US 6451681), hereinafter Greer.

Regarding claim 47, Lin (refer to Figure 1) teaches the said second contact pad (28), polymer layer (20) over said passivation layer (18), but does not position a polymer layer such that "an opening in said polymer layer exposes said second contact pad (28)". Greer teaches a top level contact pad (312) in an electronic component with a polymer layer (302) over a passivation layer (300) such that, an opening in said polymer layer exposes said second contact pad. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that an opening in said polymer layer exposes said second contact pad. The ordinary artisan would be motivated to modify Lin at least for the purpose of providing a protection layer over the pads.

Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Jiang (2003/0119299), hereinafter Jiang.

Regarding claim 51, Lin teaches substantially the claimed method but does not specifically state that forming "said second contact pad" comprises depositing "solder". Jiang teaches forming contact pads, wherein forming contact pads comprises depositing solder (para 0043, last two sentences). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that forming

said second contact pad comprises depositing solder. The ordinary artisan would be motivated to modify Lin at least for the purpose of utilizing a metal/alloy that has acceptable electrical conductivity and wets/adheres well to other interconnect materials.

Response to Arguments

Applicant's arguments with respect to claims 1-3, 5-28, 31, 40-45, 47-51 and 76-89 have been considered but are moot in view of the new ground(s) of rejection.

One of the argument still needs to be addressed as it appears there is some misunderstanding. On page 33, applicant argues regarding claim 40 that "Nakanishi et al. teach said insulating film 4 as polyimide layer of 5 micron thick, but fail to teach, hint or suggest said insulating film 4 is a passivation layer comprising nitride, as claimed in claim 40" (emphasis added). It should be noted that whereas the insulating film 4 does not comprise nitride, Nakanishi does teach a passivation layer comprising nitride. This is not shown in the Figures but is referenced in (Col. 4, lines 22-24).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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